REMARKS

Claims 1-22 and 33-34 are in the application. By this amendment claims 1 and 11 have been amended, claims 2-10 and 12-22 remain in original form, and new claims 33 and 34 have been added. Claims 23-32 were canceled without prejudice in response to a requirement for restriction.

The specification has been amended to correct errors contained therein and to provide further support for applicants claims.

Objection to Drawings Under 37 CFR 1.84(p)(4)

The drawings were objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "30" has been used to designate both VREF generator and VREF signal. This objection is respectfully traversed.

Applicants teach on page 4, lines 27-31, that voltage regulator circuits 26 and 28 receive a reference voltage signal from a reference voltage generator 30, which is activated in response to a State Machine On (SMON) signal. Typically, the reference voltage signal from reference voltage generator 30 ramps up to a desired voltage level upon beginning a program/erase operation or a program/erase verify operation. Applicants further teach on page 5, lines 7-10, that Erase/program verify circuit 34 is operable to receive the reference voltage signal from reference voltage generator 30 and generate erase verify voltage signals and program verify voltage signals, respectively, based on the reference voltage signal. What is more, applicants identify voltage reference generator (V_{REF} GENERATOR) with reference character "30" and show the connection of voltage reference generator 30 to Erase/program verify circuit 34 using a line with an arrowhead and the text "FROM V_{REF} 30." Applicants have shown the connection between voltage reference generator 30 and Erase/program verify circuit 34 using the line with the arrowhead to avoid unnecessary clutter in FIG. 1. In other words, applicants have used a line and an arrowhead labeled with the text "FROM V_{REF} 30" to promote clarity in FIG. 1. It is respectfully submitted that applicants have consistently used reference character "30" to identify the reference voltage generator and have not used reference character "30" to

designate the reference voltage signal. Accordingly, applicants believe the drawings are in conformance with 37 CFR 1.84(p)(4).

Objection to Drawings Under 37 CFR 1.84(p)(5)

The drawings were objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: SETWB, RESETWB, RFCBIT, DSIBWn, MAXCBIT, WBUFRSTB, DINDn, PZAPO, WLOAD, RFNBIT, and DLBq in Fig. 3. This objection is respectfully traversed.

It is respectfully pointed out that the reference characters RESETWB, RFCBIT, DSIBWn, MAXCBIT, WBUFRSTB, DINDn, WLOAD, RFNBIT, and DLBq appear in the description and in the drawings. In particular, these terms are mentioned in the description as follows:

RESETWB appears at least on page 9, line 10, and page 10, line 8, of the description and in FIGS. 3 and 4;

RFCBIT appears at least on page 10, line 2, of the description and in FIGS. 3 and 4;

DSIBWn appears at least on page 8, line 26, of the description and in FIGS. 3, 4, and 5;

MAXCBIT appears at least on page 9, lines 24 and 25, and page 10, lines 17 and 18, of the description and in FIGS. 3 and 4;

WBUFRSTB appears at least on page 11, line 14, of the description and in FIGS. 3 and 5;

DINDn appears at least on page 8, line 8, of the description and in FIGS. 3 and 4;

WLOAD appears at least on page 12, line 30, of the description and in FIGS. 3 and 5;

RFNBIT appears at least on page 11, line 4, and page 12, line 12, of the description and in FIGS. 2, 3, and 5; and

DLBq appears at least on page 8, lines 10 and 11, of the description and in FIG. 3.

Reference characters SETWB and PZAPO were incorrectly labeled in FIG. 3. Reference character SETWB should be SETBWB and reference character PZAPO should PZAPD. Reference character SETBWB is discussed at least on page 9, line 13, of the description and reference character PZAPD is discussed at least on page 11, line 11, of the description and shown in FIG. 5. In addition, reference characters H1 and H2, were not included in FIG. 4. Accordingly, applicants respectfully request permission to amend the drawings to replace reference characters SETWB and PZAPO in FIG. 3 with reference characters SETBWB and PZAPD, respectively, and to include reference characters H1 and H2 in FIG. 4. Support for the addition of reference character H1 can be found on page 13, lines 11-16, of the application and support for the addition of reference character H2 can be found on page 12, lines 23-26, of the application. A set of red-lined drawings are included herewith for the examiner's approval.

Objection to Drawings Under 37 CFR 1.83(a)

The drawings were objected to under 37 CFR 1.83(a). It was stated that the drawings must show every feature of the invention specified in the claims and that the features as recited in claims 1-22 must be shown or the feature(s) canceled from the claim(s). This objection is respectfully traversed.

It is respectfully pointed out that 37 CFR 1.83(a) requires that the drawing in a nonprovisional application must show every feature of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box). Applicants believe the application is in compliance with 37 CFR 1.83(a). For example, the labeled rectangular box identified by reference character 16 identifies a portion of their invention that includes memory cells, the illustration of which are not believed to be essential for a proper understanding of the invention.

Rejection of Claims 1-22 Under 35 U.S.C. § 112, First Paragraph

Claims 1-22 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The Office action alleges that the claims contain subject matter which was not described in the specification is such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This rejection is respectfully traversed.

Applicants have been requested to point out each element as recited in the claims to be read on which element as shown in the drawings and as described in the specification to help the examiner understand the subject matter of the claimed invention. Applicants teach on page 5, line 20, and continuing to page 6, line 2, that state machine 14 is operably coupled to a memory block 16 and programmed and/or configured to control the processes of storing charge on and removing charge from floating gate memory cells (not shown) of memory block 16. For example, state machine 14 controls the operation of memory block 16 in response to incoming command and control signals on control lines, such as from an associated processor (not shown). Memory block 16 includes decoders that are operable to program and erase cells of the flash memory upon receiving appropriate control signals. By way of example, memory block 16 includes a flash EEPROM comprising an array of memory cells and decoders for controlling which part of the memory array is to be accessed, such as for programming, erasing, and/or verifying operations in accordance with an embodiment of the present invention. More particularly, memory block 16 includes a core array which is made up of an M x N array of flash memory cells. A word line and control line driver provides appropriate control voltages to the core array via a plurality of word lines. Such control voltages allow data to be stored in, read from or erased from the memory cells. A bit line driver provides appropriate control voltages to and/or receives an output signal from a plurality of bit lines within the core array.

Applicants further teach on page 1, lines 20-21, that MirrorBit™ Flash memory, includes a memory cell that is essentially split into two identical (mirrored) parts where each part stores one of two independent bits. A MirrorBit™ Flash memory cell comprises a semiconductor substrate having source and drain regions and a control gate spaced apart

from the semiconductor substrate by a multilayer dielectric structure referred to as a "charge-trapping dielectric layer." A polysilicon layer is disposed over the charge-trapping dielectric layer and serves as the control gate. A MirrorBit™ Flash memory cell is programmed by applying a high voltage to the control gate and connecting the source to ground and the drain to a predetermined potential above the potential applied to the source, i.e., above ground potential. During programming, electrons are injected into and removed from the charge-trapping dielectric layer, which causes the threshold voltage, V_T, of the MirrorBit™ Flash memory cell to vary. Unlike conventional Flash memory cells, the source and drain of a MirrorBit™ Flash memory cell can be reversed during operation to permit the storing of two bits. Because this type of memory cell is capable of storing two bits, one of the bits is referred to as the normal bit and the other bit is referred to as the complementary bit.

Thus, applicants teach that memory block 16 includes an array of memory cells and that the memory cells serve as memory locations. The memory cells or memory locations are capable of storing two bits, wherein one of the bits is referred to as the normal bit and the other bit is referred to as the complementary bit.

With respect to the statement regarding readability and the drawings, it is respectfully pointed out that 37 CFR 1.83(a) states that conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box). Applicants believe that the labeled rectangular box identified by reference character 16 identifies a portion of their invention that falls within the guidelines set forth in 37 CFR 1.83(a). Accordingly, applicants believe the application as filed is in compliance with 35 USC § 112, first paragraph.

The Office action further requests clarification of the second updated latch value as recited in claim 1. Applicants teach on page 12, lines 20-22, that control signal DLBL is pulsed high to allow input data DINDn to be ORed with the logic low value appearing at node G2 to generate an updated latch value. This updated latch value is also referred to as a refresh value. Applicants teach on page 14, lines 4-6, that Control signal DLBH is pulsed high to allow input data DINDn to be ORed with the logic low value appearing at node G2

to generate an updated latch value. This updated latch value is also referred to as a refresh value. The updated latch values result from two different control signals, i.e., control signals DLBL and DLBH. Applicants believe this provides the clarification requested in the Office action.

Rejection of Claims 1-22 Under 35 U.S.C. § 102(e)

Claims 1-22 were rejected under 35 U.S.C. § 102(e) as being unpatentable over Yamaguchi et al. (U.S. Patent No. 6,754,126). This rejection is respectfully traversed.

Yamaguchi et al. teach in column 1, lines 8-10, that their invention relates to a technology to automatically perform the refresh operation in its interior without the need for a refresh request from the exterior.

Yamaguchi et al. teach in column 2, line 50, and continuing to column 3, line 43, that according to another aspect of their invention, the first and second memory blocks are structured of volatile memory cells from which data disappears over time. The second command is a refresh command generated periodically for performing refresh operation of memory cells. Therefore, the users can use the semiconductor memory without any recognition of the refresh. For example, applying their invention to the DRAM makes a refresh controller unnecessary in a system on which the DRAM is mounted. In other words, the users can use the DRAM in much the same way as the SRAM.

According to another aspect of their invention, Yamaguchi et al. an external write cycle, as a minimum interval between supplies of the write command, is set to be longer than an internal write cycle as actual write operation time to the first and second memory blocks. A refresh cycle can be inserted without fail while the write command is supplied a plurality of times. Hence, it is possible to prevent the data held in the memory cells from being destroyed, even while the write command is supplied many times. As a way of example, in a semiconductor memory of a clock synchronous type, when the external write cycle is set to n clock cycles (n is an integer equal to or greater than 1), the internal write cycle is set to n-0.5 clock cycles. In this case, when the refresh cycle is 3.5 clock cycles, one refresh cycle can be inserted during seven write operations.

According to another aspect of the semiconductor memory of Yamaguchi et al.'s invention, when the internal write cycle is set to n-0.5 clock cycles, every time the write command or the refresh command is supplied, a cycle switching circuit alternately operates first and second cycle generators to operate in synchronization with a first edge and a second edge of an external clock, respectively. The first cycle generator generates a first timing signal for performing an internal operation cycle in synchronization with the first edge of the external clock. The second cycle generator generates a second timing signal for performing the internal operation cycle in synchronization with the second edge of the external clock. The two cycle generators are used alternately to perform the write operation or the refresh operation, by which facilitates the control of performing each operation.

According to another aspect of their invention, the write control circuit includes a state control circuit. The state control circuit sequentially holds next write commands supplied during write operation to perform a write operation corresponding to one of the supplied commands which is being held after completion of the write operation. Hence, even when the refresh operation is inserted during successive write operations, it is possible to reliably perform the write operation after the first operation.

Yamaguchi et al. teach in column 3, lines 44-55, that in accordance with another aspect of their invention, when the read command is supplied to the first memory block in write operation or refresh operation, the read control circuit reproduces read data by using the data stored in the first memory blocks except for the first memory block in the operation, and the second memory block. This makes it possible to perform the read operation without a delay in the access time even when the read operation or the write operation, and the refresh operation conflict with each other inside the semiconductor memory.

Yamaguchi et al. teach in column 6, line 54, and continuing to column 7, line 21, that in accordance with another aspect of their invention, a refresh counter indicates a memory cell on which a refresh operation is to be performed, and counts up with every refresh request. Lower bit(s) of the refresh counter correspond(s) to a bank address for selecting the bank. The refresh operation is performed for each bank. Reducing the number of the refresh control circuits to concurrently operate can further decrease a peak

current during the refresh operation. Further, since the plurality of banks are refreshed alternately, generation intervals of the refresh request can be shortened as compared with the case where the same bank is successively refreshed. Therefore, even with a low operating frequency, it is possible to satisfy a necessary period for refreshing all of the memory cells. In other words, the lower limit of an operating frequency can be set to a lower value.

According to another aspect of their invention, the semiconductor memory comprises a memory core including a plurality of memory blocks for distributing and storing a plurality of bit data corresponding to the same address, and a control circuit for controlling the memory core. The control circuit is able to control refresh operations of the plurality of memory blocks independently so as to perform refresh operations on one memory block and another memory block at different timings. Independently performing the refresh operation on the plurality of memory blocks makes it possible to concurrently process an access request from the exterior and the refresh operation. That is, the refresh operation on a part of the memory blocks and an access to the other memory blocks from the exterior can be performed at the same timing. Thereby, the read operation can be realized within an access time taken for a single operation of the memory core. Namely, the read operation can be performed quickly.

Yamaguchi et al teach in column 54, lines 8-36 that the refresh request (OSC) signal generator 604 regularly outputs a pulse of a refresh request signal OSC. The internal command generator 601 outputs a signal ATD when the external command EXTC is inputted. With a case where the refresh request signal OSC and the external command EXTC overlap each other taken into consideration, a command-refresh comparator 603 always determines which of the signal ATD and the signal OSC arrives earlier.

When it is determined that the refresh request signal OSC arrives earlier, the command-refresh comparator 603 generates a refresh request signal REF. When the refresh request signal REF is inputted, a second core control signal generator 606 outputs a second core activation state signal COS2, and outputs the second core control signals COC2 (which corresponds to the second control signal SIG2 in FIG. 68) to the selector 621. Simultaneously, the refresh request signal REF is inputted to a refresh block

selector 611. The refresh block selector 611 turns one of the selecting signal SEL1 to SEL5 supplied to the selectors 621, 622 and 623 to the high level. The refresh operation is performed on only one of the blocks BLK1 to BLK5 which is thus selected by the selecting signal SEL1 to SEL5. The refresh is performed, for example, on the blocks BLK1 to BLK5 in sequence. When it is determined that the refresh request signal OSC comes later than the external command EXTC, the command-refresh comparator 603 suspends the output of the refresh request signal REF until the first core activation state signal COS1 is reset.

Yamaguchi et al. teach in column 58, line 48, and continuing to column 59, line 7, that FIG. 78 is another structural example of the word decoders 103 and the memory cells 104 which constitute one block of FIG. 68. When the mask information MSK in FIG. 73 is used, it is possible to access selectively to the upper byte and/or the lower byte. One block includes a main word decoder 1101, a sub word decoder 1102, memory cells for upper byte 1103, a sub word decoder 1104 and memory cells for lower byte 1105.

Suppose that there are four blocks BLK1 to BLK4 for storing the data of the sixteen bits at the same address. The four-bit data of the same address are stored in one block. At the same address, the upper byte is the upper eight bits and the lower byte is the lower eight bits. The memory cells 1103 store two bits of the upper byte. The memory cells 1105 store two bits of the lower byte.

The main word decoder 1101 decodes according to the row address supplied from the exterior. According to an output from the main word decoder 1101, the sub word decoder 1102 identifies the row address of the memory cell 1103. According to the output from the main word decoder 1101, the sub word decoder 1102 identifies the row address of the memory cell 1103. According to the output from the main word decoder 1101, the sub word decoder 1104 identifies the row address of the memory cell 1105. The read operation and the write operation of the upper byte and the lower byte can be performed by separate control. The refresh operations can be performed simultaneously on the memory cell 1103 and on the memory cell 1105 in one block.

Thus, Yamaguchi et al. teach a semiconductor device capable of resolving conflicts between a read command and a refresh command and between a write command and a refresh command. The semiconductor device of Yamaguchi et al. includes a

refresh counter that counts up with every refresh request which allows alternately refreshing banks thereby reducing the number of refresh control circuits, the intervals of the refresh request, and the peak current. Yamaguchi et al. further teach a semiconductor memory comprising a core having a plurality of memory blocks and performing refresh operations on one memory block and another memory block at different times. Yamaguchi et al. do not include, teach, or suggest refreshing a normal bit of a byte stored in the memory device and refreshing a complementary bit of the byte stored in the memory device.

Applicants, on the other hand, teach placing a memory system in a READ refresh mode to refresh the normal bits of the high byte during a first half of a first clock cycle; latching the refresh signal in a write latching portion during the second half of the first clock signal, refreshing the complementary bits for the entire word during the second half of the second clock signal; and refreshing the low byte of the word during a third clock signal.

Accordingly, applicants' amended claim 1 calls for, among other things, generating a first updated latch value for a normal bit of a byte, writing the first updated latch value to the first memory location during a clock cycle, generating a second updated latch value for a complementary bit of a byte, and writing the second updated latch value to the second memory location during a subsequent clock cycle. Applicants' amended claim 11, calls for, refreshing a normal bit of a byte stored in the memory device during a clock cycle and refreshing a complementary bit of the byte stored in the memory device during a different clock cycle. Support for the amended language of claims 1 and 11 can be found on page 11, line 33, and continuing to page 15, line 24, of the application. Applicants' claim 15, calls for among other things, latching a memory value in the data latch in response to the first and second control signals, performing a logic operation on the memory value and a data value to generate a refresh value, transmitting the refresh value to an output terminal of the write latch, applying the first control signal and a third control signal to the complementary data latch, latching a complementary refresh value in the complementary data latch in response to the first control signal and a third control signal, and transmitting the complementary refresh value to the output terminal of the write latch. At least these limitations of applicants' claims 1, 11, and 15 are not included

in the relied on reference of Yamaguchi et al. Because all limitations of applicants' claims 1, 11, and 15 are not included in the relied on reference of Yamaguchi et al., it cannot anticipate applicants' claim 1, 11, and 15.

Claims 2-10 depend either directly or indirectly from claim 1 and are believed allowable over the relied on reference of Yamaguchi et al. for at least the same reasons as claim 1.

Claims 12-14, 33, and 34 depend either directly or indirectly from claim 11 and are believed allowable over the relied on reference of Yamaguchi et al. for at least the same reasons as claim 11.

Claims 16-22 depend either directly or indirectly from claim 15 and are believed allowable over the relied on reference of Yamaguchi et al. for at least the same reasons as claim 15.

New Claims

New claims 33 and 34 have been added to further claim applicants' invention. New claims 33 and 34 do not introduce new subject matter.

Conclusion

No new matter is introduced by the amendments herein. Based on the foregoing, applicants believe that all claims under consideration are in condition for allowance. Reconsideration of this application is respectfully requested.

Respectfully submitted,

Dated: 5 July 2005

Rennie William Dover, Reg. No. 36,503
THE CAVANAGH LAW FIRM
1850 N. Central Avenue, Ste. 2400
Phoenix, Arizona 85004
Telephone: (602) 322-4000